Please replace page 1, lines 17-27, as follows:

Today, in the semiconductor device fabrication industry and electronics industry several trends are driving the development of new material technologies. First, devices (e.g., portable personal devices) are continuously getting smaller and requiring less power. Second, in addition to being smaller and more portable, these devices require more computational power and on-chip memory. In light of these trends, there is a need in the industry to provide a computational device that has a relatively large memory capacity and transistor functionality integrated onto the semiconductor chip. Preferably, this computational device will include a non-volatile memory so that if the battery dies, the contents of the memory will be retained. Examples of conventional non-volatile memories include electrically erasable, programmable read only memories ([~~"EEPPROM"~~] "EEPROM") and flash EEPROMs.

Please replace page 8, lines 3-16, as follows:

The capacitor dielectric layer 62 is formed over the bottom electrode 60. The capacitor dielectric layer 62 preferably is less than 150 nm thick, more preferably, is less than 100 nm thick and, most preferably, is less than 50 nm thick. Capacitor dielectric layer 62 is formed from a ferroelectric material (e.g. Pb(Zr, Ti) O_3 (PZT – lead zirconate titanate); doped PZT with donors (Nb, La, Ta), acceptors (Mn, Co, Fe, Ni, Al), and/or both; PZT doped and alloyed with $SrTiO_3$, $BaTiO_3$ or $CaTiO_3$; strontium bismuth tantalate (SBT) and other layered perovskites such as strontium bismuth niobate tantalate (SBNT); or bismuth titanate; $BaTiO_3$; $PbTiO_3$; or Bi_2TiO_3). In embodiments having a PZT capactiro dielectric layer 62, the PZT layer may be formed as described in U.S. Application Serial No. 09/702,985, filed October 31, 2000, and entitled "Method of Fabricating a Ferroelectric Memory Cell." Alternatively, the PZT capacitor dielectric layer 62 may be formed as described in U.S. Application Serial No. 09/925223, filed August 8, 2001, by Stephen R. Gilbert et al., and entitled "Forming Ferroelectric Pb(Zr,Ti)O_3 Films" [[Attorney Docket No. 10004085-1]].

Please replace page 9, lines 18-23, as follows:

Clean Replacement Paragraphs

Page 1, lines 4-12:

This application is related to U.S. Application Serial No. 09/702,985, filed October 31, 2000, and entitled "Method of Fabricating A Ferroelectric Memory Cell," which incorporated herein by reference. This application also is related to U.S. Application Serial No. 09/925,223, filed August 8, 2001, by Stephen R. Gilbert et al., and entitled "Forming Ferroelectric $Pb(Zr,Ti)O_3$ Films" and to U.S. Application Serial No. 09/925,201, filed August 8, 2001, by Stephen R. Gilbert et al., and entitled "Contamination Control for Embedded Ferroelectric Device Fabrication Processes", both of which also are incorporated herein by reference.

Page 1, lines 17-27:

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and other layered perovskites such as strontium bismuth niobate tantalate (SBNT); or bismuth titanate; $BaTiO_3$; $PbTiO_3$; or Bi_2TiO_3). In embodiments having a PZT capacitor dielectric layer 62, the PZT layer may be formed as described in U.S. Application Serial No. 09/702,985, filed October 31, 2000, and entitled "Method of Fabricating a Ferroelectric Memory Cell." Alternatively, the PZT capacitor dielectric layer 62 may be formed as described in U.S. Application Serial No. 09/925223, filed August 8, 2001, by Stephen R. Gilbert et al., and entitled "Forming Ferroelectric $Pb(Zr,Ti)O_3$ Films".

Page 9, lines 18-23:

In some embodiments, the backside and edge regions of substrate 26 are etched to reduce substantially cross-contamination by ferroelectric materials through shared equipment (e.g. steppers, metrology tools, and the like) (see, e.g. U.S. Application Serial No. 09/925,201, filed August 8, 2001, by Stephen R. Gilbert et al., and entitled "Contamination Control for Embedded Ferroelectric Device Fabrication Processes".